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Specification amendment

Correction of Figure 6 requires renumbering of A/D converter 454 into 455 and Processor 452 into 453. New corrected paragraphs follow:

[0059] Coherent receiver 400 can be calibrated digitally, as FIG. 5, or in an analog self homodyne manner, as illustrated in FIG. 6 with the calibration block marked as 446. Referring to FIG. 5, coherent receiver 400 is digitally calibrated. Coherent detector outputs 428 and 429 can be connected to two fast (symbol rate) A/D converters for further digital signal processing. Digital samples 448 and 450 are processed by processor 453.

[0060] In the analog self-homodyne implementation embodiment, illustrated in FIG. 6, coherent detector analog outputs 428 and 429 can be tapped and sampled by two A/D converters 455 and 456. The A/D outputs are directed to processor 453. These A/Ds can have bandwidths lower than the symbol rate, since they are used while keeping the symbols constant during the A/Ds integration time (training).

[0061] Processor 453 collects samples of inputs 448 and 450, and estimates their statistical properties, and performs the control algorithms as described below.